ABSTRACT

Disclosed is a signal processing apparatus for implementing a quadratic term of a second-order Volterra filter. This signal processing apparatus (10) includes a plural number of multipliers each adapted for multiplying first and second signals. Each multiplier includes one or more series-connected delay circuits, each delaying a signal output from the multiplier, by a preset time, and one or more coefficient multipliers for multiplying a signal output from each multiplier and a signal output from each delay circuit, each by a preset coefficient. A plural number n, n being an integer not less than unity, of the multipliers are connected in parallel with one another, and a k'th multiplier, k being an integer such that $1 \leq k \leq n$, uses a signal, delayed from the first signal a time equal to $(k-1)$ times by a unit time, as the second signal.